EE/CprE/Se 491 Weekly Report 7
10/25/24 - 10/31/24
sdmay25-28
Digital ASIC fabrication
Client & Advisor: Dr. Duwe

Team Members

Calvin Smith – Accelerator Design lead
Camden Fergen – DevOps, Testing, and Project lead
John – Caravel Lead
Nicholas – Harden and Verification lead
Levi – Integration Master

Weekly Summary

This week we were able to synthesize one of the soft cores. We were also able to get the datapath 1 from CPRE 381 to pass precheck, so now the goal will be to add this to the sddec24-12's project for the November deadline. This will allow us to get something physical for our presentation at the end of senior design. We also found some applications for accelerators; this will be useful when we try implementing our own custom instructions.

Pask Week Accomplishments

- Calvin:
    - Found the picorv32 processor
    - Learned the instruction interface for the pico
    - Implemented a custom byte-wise accumulate instruction
    - Made the presentation for the advisor/client meeting (goes hard)
    - Created a testbench for the pico on vivado
    - Synthesized the pico on vivado
- Camden:
    - Worked with Calvin to determine which riscv processor to use
    - Started to learn about the picorv32
    - Setup the VM to harden using openlane and efabless tooling
    - Hardened the user project example and proved it worked
    - Started to try and harden the picorv32
    - Created the lighting talked (goes hard, just not as hard as the advisor client meeting one)
- John:
    - Found some accelerator applications for us to further research

    - Researched possible custom instructions
- Levi:
    - Looked into CGRA implementations in RISC-v cpus
    - Researched similiar projects
- Nicholas:
    - Changed datapath back to 32 bits, resynthesized and ran precheck
    - Wrote comprehensive test for datapath
    - Successfully ran RTL test

Name	Individual Contribution	Hours this Week	Hours Cumulative
Calvin	-Presentation -Custom Instruction -Custom instruction testbench	12.5	48.544
Camden	-Working VM for hardening -WIP hardened picorv32 -Lighting talk pres	10	46
John	-Found accelerator applications -Research possible custom instructions	6	40
Levi	-Read 3 whitepapers	7	43
Nicholas	-Got 32-bit datapath through eFabless process. -Created comprehensive test code. -Successfully ran tests.	20	60

<u>Plans for Upcoming Week</u>

- Calvin:
    - Create a more robust testing suite for custom instructions
    - Begin work with Verilator
    - Create a template for future instruction implementation
- Camden:
    - Continue trying to harden picorv32

    - Ensure VM contains all software (i think so)
    - Understand the openlane stuff more
- John:
    - Further research accelerator applications
- Levi:
    - Define and list good applications (coming up with metrics for what good means)
- Nicholas:
    - Work with sddec24-12 to incorporate datapath into their design.
    - Help other group members with eFabless tools.

Summary of weekly advisor meeting

For this week's meeting, we met with Duwe and presented some basic questions and ideas that we wanted to clear up when searching for RISC-V cores to use. We were able to clear some things up and we ended up deciding to use LiteX and use one of the soft cores from there. We must find a well-documented, supported and open-source soft core otherwise it may become hard to implement. Instead of focusing on creating a CGRA we are going to find accelerators and then from there, work towards possibly creating a CGRA (due to its complexity it may not be feasible).